New TASCA Data Acquisition Hardware Development for the Search of Element 119 and 120

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For the search of element 119 and 120 at TASCA in year 2012 a completely new data acquisition system was developed in Experiment Electronics (EE) department of GSI. The main hardware component of the system is a FEBEX3A module (see Figure 1).

FEBEX3A is a 16 channel ADC board containing the complete control and readout logic. The ADC resolution is 12-bit and the sampling rate is 60 MSPS respectively 16.7ns per sample. The inputs of the ADCs are differential with a range of 2V (peak-peak). In front of the ADCs high performance and high rate drivers are implemented. They allow an adjusting of the gain and input impedance.

The input connector of FEBEX3A allows connecting of different piggy-boards, equipped with 16 differential analog inputs and 16 differential LVDS I/Os. For the TASCA experiment an APFEL ASIC [1] amplifier-shaper (developed in EE department) plug-in board will be used (FEBAPF).

Up to 19 FEBEX3A boards can be connected to one backplane, mounted in a standard 3HE crate. The backplane is equipped with 20 PCI-express connectors allowing a data transfer rate of 2 Gbps. An optical interface board is plugged into the first slot of the crate which allows the connection to the PCI-express interface PEXOR3. Four crates can be controlled and readout over optical cables by one PEXOR3 card, located in a standard PC.

Trigger and control signals are distributed over the backplane of the crate to all FEBEX3A modules.

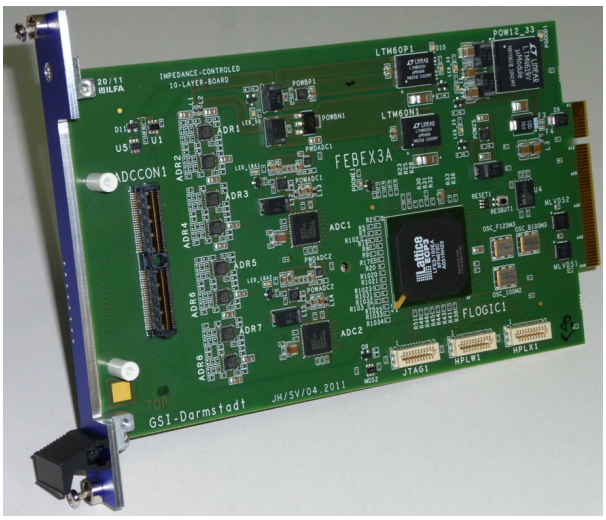

Figure 1. Photograph of FEBEX3A module.

An EXPLODER2A module serves as trigger distribution node. Up to 4 crates (1216 ADC channels) can be connected to one trigger distribution module. A multi-point LVDS standard was chosen for a trigger bus. It allows cable connection of several meters to/from up to 32 modules per chain. The interface board is equipped with a trigger-bus cable connector and allows the distribution of the trigger signals over the backplane. The complete system is in a test assembly in EE department laboratory since September 2011. One crate equipped with 6 FEBEX3A boards (96 ADC channels) was successfully tested in TASCA environment.

The logic for the FPGA chip has been programmed with Verilog HDL and VHDL. It uses GOSIP protocol with 2 modes of data transfer – address mode for read/ write access to control registers and block mode for fast

Figure 2. Photograph of FEBEX3A system.

read access to readout-buffers [2]. The 12-bit serial data from the ADCs are converted into a 12-bit parallel format and stored temporally in 16 ring-buffers with a depth of 2048. This allows the recording of ADC data up to a maximum of 34µs before a trigger occurs. When trigger signals are accepted, the data are transferred from the ring-buffers to the readout-buffers – realized as double buffers to minimize the dead time. The buffers are 32-bit in width and 4096 in depth to store ADC trace of maximum 126µs. Two different methods for signal-finding in the ADC spectra are implemented to produce self-trigger signals and to perform a data reduction on-board. One method is to find 3 consecutive samples higher than the predecessor by specified threshold. The other requires that the average of 8 samples is higher than average of 16 samples (equatable the baseline) by specified threshold with choice of 4 sampling frequency modes of 60, 30, 15 and 7.5 MHz.

[1] P. Wieczorek et al, "The APFEL-ASIC for the Silicon Strip Detector Readout at TASCA", GSI Scientific Report 2011

[2] S. Minami et al, "Design and Implementation of a Data Transfer Protocol Via Optical Fiber", IEEE Trans. Nucl. Sci., vol. 58, no. 4, p. 1816, Aug. 2011.